Course Title: Computer Architecture

Course no: CSC-201

Credit hours: 3 Full Marks: 80+20

Nature of course: Theory (3 Hrs.) Pass Marks: 32+8

Course Synopsis: This course gives the fundamental knowledge concern with the way the hardware components are connected together to form a computer system and how they interact to provide the processing needs of the user.

Goals:

- Introduces the fundamental concepts behind the design working and organization of a computer system.
- Instruction set architecture, memory hierarchies and interconnection.

Unit	Topics	Hrs.
1	**Data Representation**	**(5)**
	• Data Representation	1.5
	➢ Data Types- number systems, alphanumeric representation, complements (r's and r-1's)	
	• Fixed Point Representation	
	➢ Integer Representation	1
	➢ Arithmetic addition, subtraction, overflows.	
	➢ Decimal fixed point representation	
	• Floating Point Representation	
	• Binary and Decimal Codes	
	➢ Gray, BCD, ASSCII ,Excess-3	1
	• Error Detection code	1
	➢ Parity bit, parity checker and parity generator	0.5
2	**Micro operations**	**(5)**
	• Arithmetic Micro operations	**2**
	➢ Add micro operation, subtract micro operation	
	➢ Binary adder, binary subtractor, binary adder-subtractor ,binary incrementor,	
	➢ Arithmetic circuit	
	• Logic Micro operations	
	➢ Logic microoperations	
	➢ Implementations and application	**1**
	• Shift Microoperations	
	➢ Logical shift, circular shift, arithmetic shift.	
	➢ Combinational circuit shifter	**1**
	• Arithmetic Logic Shift Unit	**1**

3	**Fundamental of Computer Organization and Design**	**(7)**
	• Computer Register ➢ Registers for the basic computer and common bus system	**1**
	• Computer Instructions ➢ Instruction format, basic instructions, instruction set completeness, types of instructions (memory reference, register reference, i/o)	**1.5**
	• Instruction Cycle, ➢ Phases of instruction cycle ➢ Fetch & decodes ➢ Flowchart for instruction cycle	**1**
	• Input and Output and Interrupt ➢ i/o configuration, Input-output instruction ➢ Types of interrupt, Program Interrupt, interrupt cycle	**1.5**
	• Basic computer Design and Accumulator Logic ➢ Basic Hardware components ➢ Flowchart for computer operations ➢ Control logic gates ➢ Control of registers and memory ➢ Control of common bus ➢ Control of Flip flop ➢ Design of accumulator logic (control of AC register, Adder and logic circuit)	**2**
4	**Control Unit**	**5**
	• Control Memory ➢ Control word, control memory, stored program organization	**1**
	• Hardwired control ➢ Introduction, Timing and Control, Control unit of basic computer, timing signal	**1**
	• Micro programmed Control ➢ Microprogram control organization ➢ Address Sequencing o Introduction, conditional branching, Mapping of instruction, subroutines ➢ Microprograms o Microinstruction and microoperation format, Symbolic Microinstructions, Symbolic microprogram, Binary microprogram ➢ Design of Control Unit o Field decoding, Microprogram sequencer	**3**
5	**Central Processing Unit**	**6**
	• Register Organization ➢ Bus System and CPU, Control word, ALU and Microoperation for CPU	**0.5**
	• Register Stack and memory Stack ➢ LIFO and Stack Pointer, Register Stack, Memory Stack	**1**

	• One address and two address instruction ➢ Instruction Format, One address instruction, two address instruction, three address instruction and zero address instruction • Addressing Modes ➢ Introduction, Implied Mode, Immediate Mode, Register Mode, Register Indirect Mode, autoincrement/autodecrement Mode, Direct Address Mode, Indirect Address Mode, Relative Address Mode, Indexed Addressing ModeBase Register Addressing Mode • Data transfer and Manipulation ➢ Basic Operations ➢ Data Transfer Instructions ➢ Data Manipulation Instructions o Types, Arithmetic Instructions, Logical and Bit Manipulation Instruction, Shift Instruction • Introduction to RISC and CISC ➢ Introduction to RISC and CISC, Characteristics of RISC and CISC, Overlapped Register Window	**1.5** **1** **1** **1**
6	**Fixed point Computer Arithmetic**	**5**
	• Addition and Subtraction ➢ Introduction, Addition and subtraction with signed magnitude, Hardware Implementation, Hardware Algorithm ➢ Addition and subtraction with signed 2's complement • Multiplication ➢ Introduction, Hardware Implementation and Algorithm, Booth Algorithm, Array Multiplier • Division Algorithm ➢ Introduction, Hardware Implementation, Overflow, Hardware Algorithm, Restoring method, Comparison and nonrestoring Method.	**1.5** **2** **1.5**
7	**Input and Output Organization**	**(6)**
	• Introduction to Peripheral Devices ➢ I/O subsystem and peripherals • I/O interface ➢ Interface, I/O bus and interface module, Types of I/O Commands ➢ I/O and Memory bus, Isolated I/o, Memory Mapped I/O, I/O interface Unit • Direct Memory Access (DMA) ➢ Types of I/O, DMA, DMA Transfer • I/O Processor ➢ I/O Processing, CPU-IOP Communication • Data communication processor ➢ Serial and parallel Communication, data communication processor, Modes of data transfer, Protocol	**0.5** **1.5** **1.5** **1.0** **1.5**
8	**Memory Organization**	**(6)**

	• Hierarchy of Memory System ➢ Types of Memory, Sequential, Random, Memory Hierarchy • Primary and Secondary Memory ➢ Primary memory-RAM, ROM, Bootstrap Loader, RAM and ROM Chips, Memory Address Map, Memory-CPU connection ➢ Auxiliary Memory-Types, Magnetic (Tape, Disk), Optical, Semiconductor • Virtual Memory ➢ Introduction, Address space, Memory space, Address Mapping using Pages, Associative Page Table , Page Replacement • Memory Management hardware ➢ Introduction, Segmented Page Mapping, Memory Protection	**1** **1.5** **2.5** **1**

Text Books: M. Morris Mano, **Computer System Architecture**

References:

M. Morris Mano "Digital Design", Pearson Education, Third Edition

M. Morris Mano "Logic and Computer Design Fundamentals, Pearson Education, 2nd Edition Updated.