Micro-Syllabus - Digital Logic

BSc.CSIT – Second Semester
Course Title : Digital Logic
Course No. : CSC-151 **Full Marks : 60+20+20**
Credit hours : 3 **Pass Marks : 24+8+8**

Nature of course : Theory (3 Hrs.) + lab (3 Hrs)

Course Synopsis : General concepts to be used in the design and analysis of digital systems and introduces the principles of digital computer organization and design.

Goals:

- Introduce fundamentals digital logic and switching networks. Exposure of Boolean algebra and its application for circuit analysis.
- Introduction to multilevel gates networks, flip-flop, counters and logic device.

Course Contents:

Units	Topics	Hours	Remarks
1.Binary Systems	1. Digital systems ➢ Digital and Analog system ➢ Block diagram of digital computer ➢ Advantages /disadvantages of digital system	1	**7 hours**
	2. Binary Numbers ➢ Number system (binary, decimal, octal, hexadecimal), Importance of number system ➢ Number base conversion (binary to decimal, octal & hexadecimal and vice versa etc). ➢ Complements-r's, (r-1)'s ➢ Complement methods of addition/subtraction (r's & r-1's)	4	
	3. Binary systems ➢ BCD codes, error-detection codes, reflected code, alphanumeric codes (ASCIL, EBCDIC)	1	
	Integrated Circuits ➢ concept of DIP, SIMM, linear and digital ICs ➢ advantage of ICs ➢ Scale of integration- SSI, MSI, LSI,VLSI	1	
2. Boolean algebra and Logic Gates	1. Basic definition of Boolean Algebra ➢ Introduction ➢ Common postulates	1	**6 hours**

	2.Basic Theory of Boolean Algebra ➢ Duality theorem ➢ Basic theorems ➢ DeMorgans theorem		
	3. Boolean Function ➢ Boolean function and truth table ➢ Algebraic manipulation and simplification of Boolean function ➢ Complement of a function	1	
	4. Logic operations and Logic gates ➢ Logic circuits, AND, OR, NOT operation ➢ Logic gates : Basic gates, universal gates, Ex-OR, Ex-NOR, Buffer ➢ Implementation of Boolean function using gates	2	
	5. IC Digital Logic Families ➢ RTL, TTL, MOS, CMOS, I^2L ➢ Positive and negative logic, ➢ Special Characteristics-Fan out, Propagation delay, power dissipation, Noise margin ➢ Characteristics	2	
3. Simplification of Boolean Functions	1. SOP and POS ➢ SOP, POS, min- term, max-term, standard and canonical form ➢ Simplification of SOP and POS function using Boolean algebra	1 1	
	2. K-map ➢ Importance of K-map ➢ Simplification of SOP and POS form ➢ 2 and 3 variable K-map ➢ 4- variable K-map ➢ Don't care combination	3	
	3. NAND and NOR implementation ➢ NAND and NOR conversion ➢ Rules for NAND and NOR implementation ➢ Implementation of SOP and POS logic expressions using NAND, NOR and basic gates	1	
4. Combinational Logic	1. Design Procedure ➢ Definition of combinational logic circuit ➢ Design procedure ➢ Realization/Implementation	1	**6 hours**
	2. Adders / Sub-tractors ➢ Half Adder – definition, truth table, logic diagram, implementation ➢ Full Adder-definition, truth table, logic diagram, implementation ➢ Half sub – tractor ➢ Full sub-tractor	2	

	3. Code Conversion ➢ General concept ➢ Code conversion- BCD to Excess-3	1	
	4. Analysis Procedure ➢ General concept ➢ Steps in analysis ➢ Obtaining Boolean functions form logic diagram ➢ Obtaining truth table from logic diagram	1	
	5. NAND, NOR, Ex – OR circuits ➢ Concept of multi-level NAND and NOR circuits ➢ Implementation of basic operations using universal gates ➢ Block diagram method of Boolean function implementation ➢ Realization of Ex-OR using basic gates and universal gates ➢ Parity Generator, Parity Checker	1	
Unit 5. Combinational Logic with MSI and LSI	1. Adders ➢ 4-bit Parallel Binary Adder ➢ Decimal Adder –BCD adder	1	**6 hours**
	2. Magnitude Comparator ➢ Definition ➢ 4-bit Magnitude Comparator	1	
	3. Decoder ➢ Definition of Encoder and Decoder ➢ 3-to-8 line decoder	1	
	4. Multiplexers ➢ Meaning of multiplexing and de-multiplexing ➢ 4-to-1 line multiplexer	1	
	5. Read-Only-Memory (ROM) ➢ Types of ROM ➢ Combinational logic implementation of ROM	1	
	6. Programmable Logic Array (PLA) ➢ Difference between ROM and PLA ➢ Block diagram of PLA ➢ PLA Program Table ➢ Implementation of PLA	1	
Unit 6. Sequential Logic	1. Flip – Flop ➢ Definition of sequential circuit ➢ RS flip-flop, clock RS FF ➢ D-flip flop, J-K flip flop, T-flip flop, J-K Master Slave FF 2. Triggering of flip-flop ➢ Clock pulse	3 2	**8 hours**

	➢ Positive and negative edge triggering ➢ Clocked JK FF, edge triggered D-FF ➢ Direct Inputs		
	2. Design with state equations and state reduction table ➢ State table ➢ State diagram ➢ State equation ➢ State Reduction and assignment 2. Design procedure ➢ Design procedure of sequential circuits	3	
7. Registers and Counters	1. Registers ➢ Introduction to registers ➢ Shift registers – serial – in serial – out, parallel in-parallel out, serial in parallel out, parallel in serial out	1	**6 hours**
	2. Ripple Counters ➢ Definition of counter, ripple and synchronous counter ➢ A synchronous counter- BCD ripple counter, Binary ripple counter 3. Synchronous Counters ➢ Binary counters ➢ Binary up/down counter ➢ BCD counter	3	
	4. Timing Sequences ➢ Word Time generation ➢ Timing signals ➢ Johnson's counter	1	
	5. Memory Unit ➢ Introduction to memory unit ➢ Block diagram ➢ Memory address Register (MAR), Memory Buffer Register (MBR) ➢ Read/write operation ➢ Integrated-circuit memory	1	
Total hours			**45 hours**

Text Book

M., Morris "**Logic & Computer Design Fundamentals**", Pearson Education.

Question Pattern:

Long Questions: Any two from three. (10 x 2 = 20)

Short Questions: Any eight from ten (5 x 8 = 40)